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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,981	05/29/2001	Donald Lee Freeriksen	ROC9-1997-0187-US2	8068

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Steven W. Roth
IBM CORPORATION
Department 917
3605 Highway 52 North
Rochester, MN 55901-7829

EXAMINER	
TRUONG, BAO Q	
ART UNIT	**PAPER NUMBER**
2187	7

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,981	FREERKSEN ET AL.	
	Examiner	Art Unit	
	Bao Q Truong	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,10-15,17,19-21,29-34,36 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-15,17,19,29-34,36 and 38* is/are allowed.

6)☒ Claim(s) *1,2,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 7.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The examiner acknowledges the applicant's submission of the amendment dated on 26 January 2004. At this point, claims 3-9, 16, 18, 22-28, 35, and 37 have been cancelled; claims 1, 10, 12-14, 17, 19-20, 29, 32-33, 36, and 38 have been amended. There are 20 claims pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebrahim et al. (U.S. Patent No. 5,905,998).

Referring to claim 1, Ebrahim teaches a method for increasing communication efficiency in a multi-processor system (see figure 1 and "abstract"), comprising:

(1) snooping, at a processor having a transition cache (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2) and at least one level of cache associated therewith (see figure 1 and 7: element 130), a first command on a system bus, said system bus providing communication between processors in said multi-processor system, wherein said first command requesting invalidation of a cache line as monitoring a "ReadToOwn" request (see

column 35: line 48) or a "WriteInvalidate" request (see column 37: line 59) sent by another UPA master;

(2) generating a second command in response to said first command at one of said levels of cache which stores said cache line if a memory image coherency state of said cache line indicates that said cache line includes modified data, said second command instructing that said cache line be castback as generating a "Writeback" request to write a "Dirty Victim" back to main memory (see column 4: lines 18-25, and column 36: line 62);

(3) transferring said second command and said cache line from said one of said levels of cache to said transition cache in response to said first command as a command and its associated data are transferred to a queue in the interface (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(4) invalidating said cache line in each level of cache associated with said processor that stores said cache line as the System Controller requests all port invalidate the datum (see column 39: lines 4-8);

(5) snooping a system response to said first command at said processor as monitoring the System Controller's response to a "ReadToOwn" request or a "WriteInvalidate" request; and

(6) processing said second command at said processor based on said system response to said first command as writeback is cancelled (see column 21: lines 56-67, and column 37: lines 16-24) if the System Controller responds to a "ReadToOwn" request or a "WriteInvalidate" request with an "Invalidate" request (see column 38: line 59) or a "CopybackInvalidate" request (see column 40: line 18).

However, Ebrahim does not clearly teach that said processing step converts said second command to a third command in said transition cache if said system response to said first command is a retry, said third command requesting said cache line be stored in a main memory of said multi-processor system.

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the method taught by Ebrahim so that said processing step converts said second command to a third command in said transition cache if said system response to said first command is a retry, said third command requesting said cache line to be stored in main memory of said multi-processor system. This would have been obvious because Ebrahim teaches that "a dirty victim must normally be written back to main memory, except that in the present invention the write back can be cancelled if the same data block is invalidated by another data processor prior to the writeback transaction becoming active" (see column 4: lines 18-25); therefore, a dirty cache line should be written back to main memory in order to maintain coherency.

As to claim 2, Ebrahim further teaches that said processing step discards said second command and said cache line from said transition cache when said system response to said first command is not a retry as writeback is cancelled (see column 21: lines 56-67, and column 37: lines 16-24) if the System Controller responds to a "ReadToOwn" request or a "WriteInvalidate" request with an "Invalidate" request or a "CopybackInvalidate" request.

Referring to claim 20, Ebrahim discloses a multi-processor system (see figure 1 and "abstract"), comprising:

(1) at least first and second processors (see figures 1 and 2: elements 102);

(2) a system bus providing communication between said first and second processors (see figures 1 and 2: elements 116 and 114);

(3) a bus arbiter generating system response to commands on said system bus (see figures 1 and 2: element 110); and wherein

(4) said first processor has at least one level of cache associated therewith (see figure 1 and 7: element 130), a system bus controller controlling communication between said first processor and said system bus (see figures 4 and 7: element 104), and a transition cache serving as an interface between each level of cache and said system bus controller (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2);

(5) one of said levels of cache associated with said first processor stores a cache lines having a memory coherency image state indicating that said cache line includes modified data (see figure 10A, column 4: lines 18-28 and line 48), and generates a castback command and transfer said castback command and a copy of said cache lines to said transition cache when said first processor snoops a first command on said system bus that requests invalidation of said cache line as generating a "Writeback" request to write a "Dirty Victim" back to main memory (see column 4: lines 18-25, and column 36: lines 62); and as a command and its associated data are transferred to a queue in the interface (see figure 4: element 150 and 152, column 11: lines 62-67, and column 12: lines 1-2); and

(6) each level of cache associated with said first processor that stores said cache line invalidates said cache line prior to said first processor snooping a system response to said first command as the System Controller requests all port invalidate the datum (see column 39: lines 4-8); and as monitoring the System Controller's response to a "ReadToOwn" request or a "WriteInvalidate" request.

However, Ebrahim does not clearly disclose that said transition cache converts said castback command to a second command if said system response to said first command is a retry, said second command requesting said cache line be stored in a main memory of said multi-processor system.

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the system taught by Ebrahim so that said transition cache converts said castback command to a second command if said system response to said first command is a retry, said second command requesting said cache line be stored in a main memory of said multi-processor system. This would have been obvious because Ebrahim discloses that "a dirty victim must normally be written back to main memory, except that in the present invention the write back can be cancelled if the same data block is invalidated by another data processor prior to the writeback transaction becoming active" (see column 4: lines 18-25); therefore, a dirty cache line should be written back to main memory to maintain coherency.

As to claim 21, Ebrahim discloses that said transition cache discards said castback and said cache line when said system response to said first command is not a retry as writeback is cancelled (see column 21: lines 56-67, and column 37: lines 16-24) if the System Controller responds to a "ReadToOwn" request or a "WriteInvalidate" request with an "Invalidate" request or a "CopybackInvalidate" request.

Response to Arguments

4. Applicant's arguments regarding to amended claims 1 and 20 have been fully considered but they are not persuasive.

On page 15, the fifth paragraph, the applicant argues that "Ebrahim does not disclose any capability to cast back the modified cache line to memory if the invalidation command **does not** complete". The examiner disagrees and directs the applicant's attention to column 4: lines 18-25 where Ebrahim discloses that the dirty (modified) cache line should be written (casted) back to main memory. An exception only occurs if the data block (in the cache line) is invalidated **prior to** the writeback transaction becoming active; that means the writeback **can be** cancelled **only if** the invalidation command **completes**. Amended claims 1 and 20 suggest executing the cast back command (the third command) **only if** the invalidation command (the first command) **does not** complete (retry). As mentioned above, Ebrahim clearly suggests this limitation.

On page 16, the first paragraph, the applicant argues that, in Ebrahim teaching, "if the data block is invalidated, write back is impossible". The examiner disagrees and directs the applicant's attention to column 4: lines 18-25 where Ebrahim suggests that writeback **can be**

cancelled if the data block is invalidated. Ebrahim's suggestion **does not** mean that write back is impossible if data block is invalidated. Furthermore, the applicant argues that "in accordance with applicant's invention, the data block can still be invalidate, and yet written back". The examiner disagrees and directs the applicant's attention to the language of amended claims 1 and 20 where the applicant suggests writing back the data block (cache line) **only if** the invalidation command (the first command) **does not** complete (retry). What happens after the retry (for the invalidation command) completes **is not** discussed in the language of amended claims 1 and 20.

Allowable Subject Matter

5. Claims 10-15, 17, 19, 29-34, 36, and 38 are allowed.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (703) 308-7090. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

BAO QUOC TRUONG

BT
Patent Examiner
22 March 2004

Donald Sparks
Supervisory Patent Examiner
Technology Center 2100